Shine Plus User manual Addendum for

ARTITEC E Plan Coaches

Functions and Output mapping

The usable functions for the Shine Plus Artitec E Plan lighting boards are F0, F1-F16.

The on board decoder has a total of 16 outputs. The LED arrangement is depending on the model (BDAD, CDBD, POST or CKDRD). The outputs Out14/Out15 are used for front/rear tail lights in each of the models. The other LED assignment is presented in the following pages.

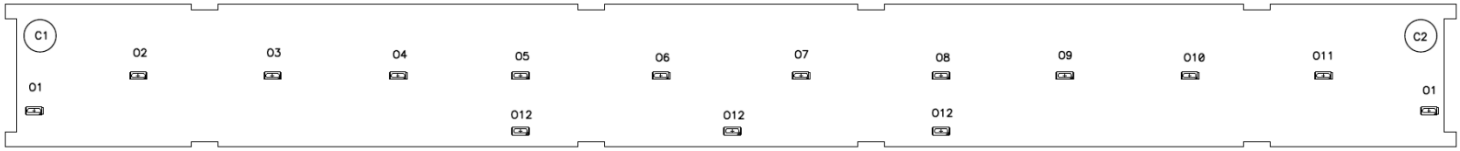
For every function mapping 4 CVs are required. Each of the functions is using 2 CVs for forward direction mapping and 2 CVs for the reverse direction mapping of the possible 16 outputs. The 4 CV groups are found in the CV table in successive order for every function. Setting different output mapping for forward and reverse direction for a function (in the corresponding CVs) will allow switching on/off different outputs (LEDs) for forward and reverse direction of travel.

The order of the 4 CVs are:
1st CV: forward direction for outputs 1-8 (bits 0-7)
2nd CV: forward direction for outputs 9-16 (bits 0-7)
3rd CV: reverse direction for outputs 1-8 (bits 0-7)
4th CV: reverse direction for outputs 9-16 (bits 0-7)

In the illustrations LEDs having the same number (starting with O..) are connected to the same output. They are controlled together. When an output is activated by a function, all LEDs connected to that output will be activated. This is the case of the corridor lighting in all models.

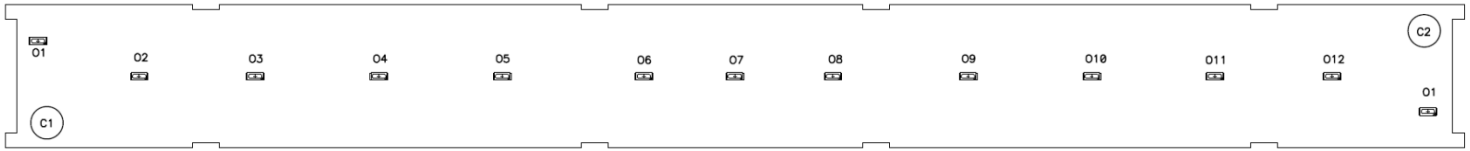
LEDs to Output assignments

(LED side view of the printed circuit board)



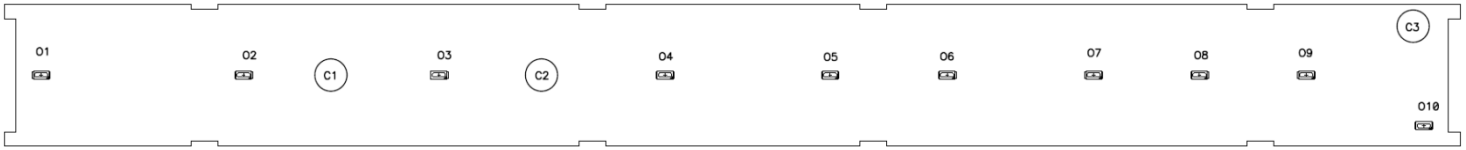
BDAD

(Outputs/ LEDs 13 and 16 not used)



CDBD

(Outputs/ LEDs 13 and 16 not used)



POST

(Outputs/ LEDs 11, 12, 13 and 16 not used)

CKDRD

(Outputs/ LEDs 12, 13 and 16 not used)

CV TABLE

The default values are referring to the POST wagon. For the other models the default values might be different.

CV	Default value	Value Range	Description
1	3	0-127	Decoder Address Short, 7 bits
7	4	-	Software Version (only readable)
8	78	-	Manufactured ID/RESET (readable 78 = train-O-matic, any written value will reset the decoder to the factory default values
13	0	0-255	Analog Mode, Alternate Mode Function Status F1-F8 Bit 0 = 0(0): F1 not active in Analog mode = 1(1): F1 active in Analog mode Bit 1 = 0(0): F2 not active in Analog mode = 1(2): F2 active in Analog mode Bit 2 = 0(0): F3 not active in Analog mode = 1(4): F3 active in Analog mode Bit 3 = 0(0): F4 not active in Analog mode = 1(8): F4 active in Analog mode Bit 4 = 0(0): F5 not active in Analog mode = 1(16): F5 active in Analog mode

			Bit 5 = 0(0): F6 not active in Analog mode = 1(32): F6 active in Analog mode Bit 6 = 0(0): F7 not active in Analog mode = 1(64) F7 active in Analog mode Bit 7 = 0(0): F8 not active in Analog mode = 1(255): F8 active in Analog mode
14	3= 1+ 2	0-255	Analog Mode, Alternate Mode Function. Status F0f,F0r, F9-F14, Bit 0 = 0(0): F0f not active in Analog mode = 1(1): F0f active in Analog mode Bit 1 = 0(0): F0r not active in Analog mode = 1(2): F0r active in Analog mode Bit 2 = 0(0): F9 not active in Analog mode = 1(4): F9 active in Analog mode Bit 3 = 0(0): F10 not active in Analog mode = 1(8): F10 active in Analog mode Bit 4 = 0(0): F11 not active in Analog mode = 1(16): F11 active in Analog mode Bit 5 = 0(0): F12 not active in Analog mode = 1(32): F12 active in Analog mode Bit 6 = 0(0): F13 not active in Analog mode = 1(64) F13 active in Analog mode Bit 7 = 0(0): F14 not active in Analog mode = 1(255): F14 active in Analog mode

15	0	0-7	LockValue: Enter the value to match Lock ID in CV16 to unlock CV programming. No action and ACK will be performed by the decoder when LockValue is different from LockID. In this situation only CV15 write is allowed.
16	0	0-7	LockID: To prevent accidental programming use unique ID number for decoders with same address (0..7) 1-loco decoder, 2-sound decoder, 3-function decoder, …
17	192	192-255	Extended Address, Address High
18	3	0-255	Extended Address, Address Low
19	0	0-127	Consist Address If CV #19 > 0: Speed and direction is governed by this consist address (not the individual address in CV #1 or #17+18); functions are controlled by either the consist address or individual address, see CV"s #21 + 22.
21	0	0-255	Functions defined here will be controlled by the consist address. Bit 0 = 0(0): F1 controlled by individual address = 1(1): …. by consist address Bit 1 = 0(0): F2 controlled by individual address = 1(2): …. by consist address Bit 2 = 0(0): F3 controlled by individual address = 1(4): …. by consist address Bit 3 = 0(0): F4 controlled by individual address = 1(8): …. by consist address

			Bit 4 = 0(0): F5 controlled by individual address = 1(16): …. by consist address Bit 5 = 0(0): F6 controlled by individual address = 1(32): …. by consist address Bit 6 = 0(0): F7 controlled by individual address = 1(64): …. by consist address Bit 7 = 0(0): F8 controlled by individual address = 1(255): …. by consist address
22	0	0-63	Functions defined here will be controlled by the consist address. Bit 0 = 0(0): F0 (forw.) controlled by individual address = 1(1): …. by consist address Bit 1 = 0 (0): F0 (rev.) controlled by individual address = 1(2): …. by consist address Bit 2 = 0(0): F9 controlled by individual address = 1(4): …. by consist address Bit 3 = 0(0): F10 controlled by individual address = 1(8): …. by consist address Bit 4 = 0(0): F11 controlled by individual address = 1(16): …. by consist address Bit 5 = 0(0): F12 controlled by individual address = 1(32): …. by consist address
29	6=	0-63	Configuration Data Bit 0 = 0(0): Locomotive Direction normal

	2+ 4		= 1(1): Locomotive Direction reversed Bit 1 = 0(0): 14 speed steps = 1(2): 28 /128 speed steps Bit 2 = 0(0): Power Source Conversion NMRA Digital Only (only DCC) = 1(4): Power Source Conversion Enabled (DC + DCC) Bit 3-Not Used Bit 4 = 0(0): speed table set by configuration variables #2,#5, and #6 = 1(16): Speed Table set by configuration variables #66-#95 Bit 5 = 0(0): one byte addressing (short addressing) = 1(32): two byte addressing (extended/long addressing) Bit 6 -Not Used Bit 7 -Not Used
30	0	0/1	Error CV. If the read out value is "1", an overcurrent event occurred since the last reset. The value can be cleared with programming "0" to CV30
33	255= 1+ 2+ 4+ 8+	0-255	F0, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F0 forward = 1(1): Out1 active on F0 forward Bit 1 = 0(0): Out2 not active on F0 forward = 1(2): Out2 active on F0 forward Bit 2 = 0(0): Out3 not active on F0 forward = 1(4): Out3 active on F0 forward Bit 3 = 0(0): Out4 not active on F0 forward = 1(8): Out4 active on F0 forward

	16+ 32+ 64+ 128		Bit 4 = 0(0): Out5 not active on F0 forward = 1(16): Out5 active on F0 forward Bit 5 = 0(0): Out6 not active on F0 forward = 1(32): Out6 active on F0 forward Bit 6 = 0(0): Out7 not active on F0 forward = 1(64): Out7 active on F0 forward Bit 7 = 0(0): Out8 not active on F0 forward = 1(128): Out8 active on F0 forward
34	31= 1+ 2+ 4+ 8+ 16+	0-255	F0, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F0 forward = 1(1): Out9 active on F0 forward Bit 1 = 0(0): Out10 not active on F0 forward = 1(2): Out10 active on F0 forward Bit 2 = 0(0): Out11 not active on F0 forward = 1(4): Out11 active on F0 forward Bit 3 = 0(0): Out12 not active on F0 forward = 1(8): Out12 active on F0 forward Bit 4 = 0(0): Out13 not active on F0 forward = 1(16): Out13 active on F0 forward Bit 5 = 0(0): Out14 not active on F0 forward = 1(32): Out14 active on F0 forward Bit 6 = 0(0): Out15 not active on F0 forward = 1(64): Out15 active on F0 forward Bit 7 = 0(0): Out16 not active on F0 forward

			= 1(128): Out16 active on F0 forward
35	255= 1+ 2+ 4+ 8+ 16+ 32+ 64+ 128	0-255	F0, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F0 backward = 1(1): Out1 active on F0 backward Bit 1 = 0(0): Out2 not active on F0 backward = 1(2): Out2 active on F0 backward Bit 2 = 0(0): Out3 not active on F0 backward = 1(4): Out3 active on F0 backward Bit 3 = 0(0): Out4 not active on F0 backward = 1(8): Out4 active on F0 backward Bit 4 = 0(0): Out5 not active on F0 backward = 1(16): Out5 active on F0 backward Bit 5 = 0(0): Out6 not active on F0 backward = 1(32): Out6 active on F0 backward Bit 6 = 0(0): Out7 not active on F0 backward = 1(64): Out7 active on F0 backward Bit 7 = 0(0): Out8 not active on F0 backward = 1(128): Out8 active on F0 backward
36	31= 1+ 2+	0-255	F0, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F0 backward = 1(1): Out9 active on F0 backward Bit 1 = 0(0): Out10 not active on F0 backward = 1(2): Out10 active on F0 backward Bit 2 = 0(0): Out11 not active on F0 backward

	4+ 8+ 16+		= 1(4): Out11 active on F0 backward Bit 3 = 0(0): Out12 not active on F0 backward = 1(8): Out12 active on F0 backward Bit 4 = 0(0): Out13 not active on F0 backward = 1(16): Out13 active on F0 backward Bit 5 = 0(0): Out14 not active on F0 backward = 1(32): Out14 active on F0 backward Bit 6 = 0(0): Out15 not active on F0 backward = 1(64): Out15 active on F0 backward Bit 7 = 0(0): Out16 not active on F0 backward = 1(128): Out16 active on F0 backward
37	240= 16+ 32+	0-255	F1, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F1 forward = 1(1): Out1 active on F1 forward Bit 1 = 0(0): Out2 not active on F1 forward = 1(2): Out2 active on F1 forward Bit 2 = 0(0): Out3 not active on F1 forward = 1(4): Out3 active on F1 forward Bit 3 = 0(0): Out4 not active on F1 forward = 1(8): Out4 active on F1 forward Bit 4 = 0(0): Out5 not active on F1 forward = 1(16): Out5 active on F1 forward Bit 5 = 0(0): Out6 not active on F1 forward = 1(32): Out6 active on F1 forward

	64+ 128		Bit 6 = 0(0): Out7 not active on F1 forward = 1(64): Out7 active on F1 forward Bit 7 = 0(0): Out8 not active on F1 forward = 1(128): Out8 active on F1 forward
38	1 1	0-255	F1, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F1 forward = 1(1): Out9 active on F1 forward Bit 1 = 0(0): Out10 not active on F1 forward = 1(2): Out10 active on F1 forward Bit 2 = 0(0): Out11 not active on F1 forward = 1(4): Out11 active on F1 forward Bit 3 = 0(0): Out12 not active on F1 forward = 1(8): Out12 active on F1 forward Bit 4 = 0(0): Out13 not active on F1 forward = 1(16): Out13 active on F1 forward Bit 5 = 0(0): Out14 not active on F1 forward = 1(32): Out14 active on F1 forward Bit 6 = 0(0): Out15 not active on F1 forward = 1(64): Out15 active on F1 forward Bit 7 = 0(0): Out16 not active on F1 forward = 1(128): Out16 active on F1 forward
39	240=	0-255	F1, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F1 backward = 1(1): Out1 active on F1 backward

	      16+ 32+ 64+ 128		Bit 1 = 0(0): Out2 not active on F1 backward = 1(2): Out2 active on F1 backward Bit 2 = 0(0): Out3 not active on F1 backward = 1(4): Out3 active on F1 backward Bit 3 = 0(0): Out4 not active on F1 backward = 1(8): Out4 active on F1 backward Bit 4 = 0(0): Out5 not active on F1 backward = 1(16): Out5 active on F1 backward Bit 5 = 0(0): Out6 not active on F1 backward = 1(32): Out6 active on F1 backward Bit 6 = 0(0): Out7 not active on F1 backward = 1(64): Out7 active on F1 backward Bit 7 = 0(0): Out8 not active on F1 backward = 1(128): Out8 active on F1 backward
40	1 1	0-255	F1, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F1 backward = 1(1): Out9 active on F1 backward Bit 1 = 0(0): Out10 not active on F1 backward = 1(2): Out10 active on F1 backward Bit 2 = 0(0): Out11 not active on F1 backward = 1(4): Out11 active on F1 backward Bit 3 = 0(0): Out12 not active on F1 backward = 1(8): Out12 active on F1 backward Bit 4 = 0(0): Out13 not active on F1 backward

			= 1(16): Out13 active on F1 backward Bit 5 = 0(0): Out14 not active on F1 backward = 1(32): Out14 active on F1 backward Bit 6 = 0(0): Out15 not active on F1 backward = 1(64): Out15 active on F1 backward Bit 7 = 0(0): Out16 not active on F1 backward = 1(128): Out16 active on F1 backward
41	15= 1+ 2+ 4+ 8	0-255	F2 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F2 = 1(1): Out1 active on F2 Bit 1 = 0(0): Out2 not active on F2 = 1(2): Out2 active on F2 Bit 2 = 0(0): Out3 not active on F2 = 1(4): Out3 active on F2 Bit 3 = 0(0): Out4 not active on F2 = 1(8): Out4 active on F2 Bit 4 = 0(0): Out5 not active on F2 = 1(16): Out5 active on F2 Bit 5 = 0(0): Out6 not active on F2 = 1(32): Out6 active on F2 Bit 6 = 0(0): Out7 not active on F2 = 1(64): Out7 active on F2 Bit 7 = 0(0): Out8 not active on F2 = 1(128): Out8 active on F2

42	22= 2+ 4+ 16	0-255	F2 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F2 = 1(1): Out9 active on F2 Bit 1 = 0(0): Out10 not active on F2 = 1(2): Out10 active on F2 Bit 2 = 0(0): Out11 not active on F2 = 1(4): Out11 active on F2 Bit 3 = 0(0): Out12 not active on F2 = 1(8): Out12 active on F2 Bit 4 = 0(0): Out13 not active on F2 = 1(16): Out13 active on F2 Bit 5 = 0(0): Out14 not active on F2 = 1(32): Out14 active on F2 Bit 6 = 0(0): Out15 not active on F2 = 1(64): Out15 active on F2 Bit 7 = 0(0): Out16 not active on F2 = 1(128): Out16 active on F2
43	15= 1+ 2+ 4+	0-255	F2 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F2 = 1(1): Out1 active on F2 Bit 1 = 0(0): Out2 not active on F2 = 1(2): Out2 active on F2 Bit 2 = 0(0): Out3 not active on F2 = 1(4): Out3 active on F2

	8		Bit 3 = 0(0): Out4 not active on F2 = 1(8): Out4 active on F2 Bit 4 = 0(0): Out5 not active on F2 = 1(16): Out5 active on F2 Bit 5 = 0(0): Out6 not active on F2 = 1(32): Out6 active on F2 Bit 6 = 0(0): Out7 not active on F2 = 1(64): Out7 active on F2 Bit 7 = 0(0): Out8 not active on F2 = 1(128): Out8 active on F2
44	22= 2+ 4+ 16	0-255	F2 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F2 = 1(1): Out9 active on F2 Bit 1 = 0(0): Out10 not active on F2 = 1(2): Out10 active on F2 Bit 2 = 0(0): Out11 not active on F2 = 1(4): Out11 active on F2 Bit 3 = 0(0): Out12 not active on F2 = 1(8): Out12 active on F2 Bit 4 = 0(0): Out13 not active on F2 = 1(16): Out13 active on F2 Bit 5 = 0(0): Out14 not active on F2 = 1(32): Out14 active on F2 Bit 6 = 0(0): Out15 not active on F2

			= 1(64): Out15 active on F2 Bit 7 = 0(0): Out16 not active on F2 = 1(128): Out16 active on F2
45	80	0-255	F3 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F3 = 1(1): Out1 active on F3 Bit 1 = 0(0): Out2 not active on F3 = 1(2): Out2 active on F3 Bit 2 = 0(0): Out3 not active on F3 = 1(4): Out3 active on F3 Bit 3 = 0(0): Out4 not active on F3 = 1(8): Out4 active on F3 Bit 4 = 0(0): Out5 not active on F3 = 1(16): Out5 active on F3 Bit 5 = 0(0): Out6 not active on F3 = 1(32): Out6 active on F3 Bit 6 = 0(0): Out7 not active on F3 = 1(64): Out7 active on F3 Bit 7 = 0(0): Out8 not active on F3 = 1(128): Out8 active on F3
46	64=	0-255	F3 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F3 = 1(1): Out9 active on F3 Bit 1 = 0(0): Out10 not active on F3

	64		= 1(2): Out10 active on F3 Bit 2 = 0(0): Out11 not active on F3 = 1(4): Out11 active on F3 Bit 3 = 0(0): Out12 not active on F3 = 1(8): Out12 active on F3 Bit 4 = 0(0): Out13 not active on F3 = 1(16): Out13 active on F3 Bit 5 = 0(0): Out14 not active on F3 = 1(32): Out14 active on F3 Bit 6 = 0(0): Out15 not active on F3 = 1(64): Out15 active on F3 Bit 7 = 0(0): Out16 not active on F3 = 1(128): Out16 active on F3
47	10	0-255	F3 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F3 = 1(1): Out1 active on F3 Bit 1 = 0(0): Out2 not active on F3 = 1(2): Out2 active on F3 Bit 2 = 0(0): Out3 not active on F3 = 1(4): Out3 active on F3 Bit 3 = 0(0): Out4 not active on F3 = 1(8): Out4 active on F3 Bit 4 = 0(0): Out5 not active on F3 = 1(16): Out5 active on F3

			Bit 5 = 0(0): Out6 not active on F3 = 1(32): Out6 active on F3 Bit 6 = 0(0): Out7 not active on F3 = 1(64): Out7 active on F3 Bit 7 = 0(0): Out8 not active on F3 = 1(128): Out8 active on F3
48	0	0-255	F3 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F3 = 1(1): Out9 active on F3 Bit 1 = 0(0): Out10 not active on F3 = 1(2): Out10 active on F3 Bit 2 = 0(0): Out11 not active on F3 = 1(4): Out11 active on F3 Bit 3 = 0(0): Out12 not active on F3 = 1(8): Out12 active on F3 Bit 4 = 0(0): Out13 not active on F3 = 1(16): Out13 active on F3 Bit 5 = 0(0): Out14 not active on F3 = 1(32): Out14 active on F3 Bit 6 = 0(0): Out15 not active on F3 = 1(64): Out15 active on F3 Bit 7 = 0(0): Out16 not active on F3 = 1(128): Out16 active on F3
49	0	0-255	F4 mapping, Forward move mapping, low byte

			Bit 0 = 0(0): Out1 not active on F4 = 1(1): Out1 active on F4 Bit 1 = 0(0): Out2 not active on F4 = 1(2): Out2 active on F4 Bit 2 = 0(0): Out3 not active on F4 = 1(4): Out3 active on F4 Bit 3 = 0(0): Out4 not active on F4 = 1(8): Out4 active on F4 Bit 4 = 0(0): Out5 not active on F4 = 1(16): Out5 active on F4 Bit 5 = 0(0): Out6 not active on F4 = 1(32): Out6 active on F4 Bit 6 = 0(0): Out7 not active on F4 = 1(64): Out7 active on F4 Bit 7 = 0(0): Out8 not active on F4 = 1(128): Out8 active on F4
50	0	0-255	F4 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F4 = 1(1): Out9 active on F4 Bit 1 = 0(0): Out10 not active on F4 = 1(2): Out10 active on F4 Bit 2 = 0(0): Out11 not active on F4 = 1(4): Out11 active on F4 Bit 3 = 0(0): Out12 not active on F4

			= 1(8): Out12 active on F4 Bit 4 = 0(0): Out13 not active on F4 = 1(16): Out13 active on F4 Bit 5 = 0(0): Out14 not active on F4 = 1(32): Out14 active on F4 Bit 6 = 0(0): Out15 not active on F4 = 1(64): Out15 active on F4 Bit 7 = 0(0): Out16 not active on F4 = 1(128): Out16 active on F4
51	0	0-255	F4 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F4 = 1(1): Out1 active on F4 Bit 1 = 0(0): Out2 not active on F4 = 1(2): Out2 active on F4 Bit 2 = 0(0): Out3 not active on F4 = 1(4): Out3 active on F4 Bit 3 = 0(0): Out4 not active on F4 = 1(8): Out4 active on F4 Bit 4 = 0(0): Out5 not active on F4 = 1(16): Out5 active on F4 Bit 5 = 0(0): Out6 not active on F4 = 1(32): Out6 active on F4 Bit 6 = 0(0): Out7 not active on F4 = 1(64): Out7 active on F4

			Bit 7 = 0(0): Out8 not active on F4 = 1(128): Out8 active on F4
52	32= 32	0-255	F4 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F4 = 1(1): Out9 active on F4 Bit 1 = 0(0): Out10 not active on F4 = 1(2): Out10 active on F4 Bit 2 = 0(0): Out11 not active on F4 = 1(4): Out11 active on F4 Bit 3 = 0(0): Out12 not active on F4 = 1(8): Out12 active on F4 Bit 4 = 0(0): Out13 not active on F4 = 1(16): Out13 active on F4 Bit 5 = 0(0): Out14 not active on F4 = 1(32): Out14 active on F4 Bit 6 = 0(0): Out15 not active on F4 = 1(64): Out15 active on F4 Bit 7 = 0(0): Out16 not active on F4 = 1(128): Out16 active on F4
53	0	0-255	F5 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F5 = 1(1): Out1 active on F5 Bit 1 = 0(0): Out2 not active on F5 = 1(2): Out2 active on F5

			Bit 2 = 0(0): Out3 not active on F5 = 1(4): Out3 active on F5 Bit 3 = 0(0): Out4 not active on F5 = 1(8): Out4 active on F5 Bit 4 = 0(0): Out5 not active on F5 = 1(16): Out5 active on F5 Bit 5 = 0(0): Out6 not active on F5 = 1(32): Out6 active on F5 Bit 6 = 0(0): Out7 not active on F5 = 1(64): Out7 active on F5 Bit 7 = 0(0): Out8 not active on F5 = 1(128): Out8 active on F5
54	0	0-255	F5 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F5 = 1(1): Out9 active on F5 Bit 1 = 0(0): Out10 not active on F5 = 1(2): Out10 active on F5 Bit 2 = 0(0): Out11 not active on F5 = 1(4): Out11 active on F5 Bit 3 = 0(0): Out12 not active on F5 = 1(8): Out12 active on F5 Bit 4 = 0(0): Out13 not active on F5 = 1(16): Out13 active on F5 Bit 5 = 0(0): Out14 not active on F5

			= 1(32): Out14 active on F5 Bit 6 = 0(0): Out15 not active on F5 = 1(64): Out15 active on F5 Bit 7 = 0(0): Out16 not active on F5 = 1(128): Out16 active on F5
55	0	0-255	F5 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F5 = 1(1): Out1 active on F5 Bit 1 = 0(0): Out2 not active on F5 = 1(2): Out2 active on F5 Bit 2 = 0(0): Out3 not active on F5 = 1(4): Out3 active on F5 Bit 3 = 0(0): Out4 not active on F5 = 1(8): Out4 active on F5 Bit 4 = 0(0): Out5 not active on F5 = 1(16): Out5 active on F5 Bit 5 = 0(0): Out6 not active on F5 = 1(32): Out6 active on F5 Bit 6 = 0(0): Out7 not active on F5 = 1(64): Out7 active on F5 Bit 7 = 0(0): Out8 not active on F5 = 1(128): Out8 active on F5
56	0	0-255	F5 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F5

			= 1(1): Out9 active on F5 Bit 1 = 0(0): Out10 not active on F5 = 1(2): Out10 active on F5 Bit 2 = 0(0): Out11 not active on F5 = 1(4): Out11 active on F5 Bit 3 = 0(0): Out12 not active on F5 = 1(8): Out12 active on F5 Bit 4 = 0(0): Out13 not active on F5 = 1(16): Out13 active on F5 Bit 5 = 0(0): Out14 not active on F5 = 1(32): Out14 active on F5 Bit 6 = 0(0): Out15 not active on F5 = 1(64): Out15 active on F5 Bit 7 = 0(0): Out16 not active on F5 = 1(128): Out16 active on F5
57	0	0-255	F6 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F6 = 1(1): Out1 active on F6 Bit 1 = 0(0): Out2 not active on F6 = 1(2): Out2 active on F6 Bit 2 = 0(0): Out3 not active on F6 = 1(4): Out3 active on F6 Bit 3 = 0(0): Out4 not active on F6 = 1(8): Out4 active on F6

			Bit 4 = 0(0): Out5 not active on F6 = 1(16): Out5 active on F6 Bit 5 = 0(0): Out6 not active on F6 = 1(32): Out6 active on F6 Bit 6 = 0(0): Out7 not active on F6 = 1(64): Out7 active on F6 Bit 7 = 0(0): Out8 not active on F6 = 1(128): Out8 active on F6
58	0	0-255	F6 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F6 = 1(1): Out9 active on F6 Bit 1 = 0(0): Out10 not active on F6 = 1(2): Out10 active on F6 Bit 2 = 0(0): Out11 not active on F6 = 1(4): Out11 active on F6 Bit 3 = 0(0): Out12 not active on F6 = 1(8): Out12 active on F6 Bit 4 = 0(0): Out13 not active on F6 = 1(16): Out13 active on F6 Bit 5 = 0(0): Out14 not active on F6 = 1(32): Out14 active on F6 Bit 6 = 0(0): Out15 not active on F6 = 1(64): Out15 active on F6 Bit 7 = 0(0): Out16 not active on F6

			= 1(128): Out16 active on F6
59	0	0-255	F6 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F6 = 1(1): Out1 active on F6 Bit 1 = 0(0): Out2 not active on F6 = 1(2): Out2 active on F6 Bit 2 = 0(0): Out3 not active on F6 = 1(4): Out3 active on F6 Bit 3 = 0(0): Out4 not active on F6 = 1(8): Out4 active on F6 Bit 4 = 0(0): Out5 not active on F6 = 1(16): Out5 active on F6 Bit 5 = 0(0): Out6 not active on F6 = 1(32): Out6 active on F6 Bit 6 = 0(0): Out7 not active on F6 = 1(64): Out7 active on F6 Bit 7 = 0(0): Out8 not active on F6 = 1(128): Out8 active on F6
60	0	0-255	F6 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F6 = 1(1): Out9 active on F6 Bit 1 = 0(0): Out10 not active on F6 = 1(2): Out10 active on F6 Bit 2 = 0(0): Out11 not active on F6

			= 1(4): Out11 active on F6 Bit 3 = 0(0): Out12 not active on F6 = 1(8): Out12 active on F6 Bit 4 = 0(0): Out13 not active on F6 = 1(16): Out13 active on F6 Bit 5 = 0(0): Out14 not active on F6 = 1(32): Out14 active on F6 Bit 6 = 0(0): Out15 not active on F6 = 1(64): Out15 active on F6 Bit 7 = 0(0): Out16 not active on F6 = 1(128): Out16 active on F6
61	0	0-3	MM multi addres mode 0 – respond only to base address from CV1 (F0 … F4) 1 – respond even to base address + 1 (F5 … F8) 2 - respond even to base address + 2 (F9 … F12) 3 - respond even to base address + 3 (F13 … F16)
62	0	0-1	Digital reception mode, it's set automatically, don't need to be modified, can be just read: 0 – DCC 1 - MM

105	0	0-255	USER data
106	0	0-255	USER data
112	15	1-127	FadeIN AUX Light Effect Fade ON, ex.:1=8ms, 15=120ms 125=1000ms
113	3	1-127	FadeOUT AUX Light Effect Fade OFF
114	3	0-7	Delay, Flourescent Tube Start, Blinking Delay 1-8 delay step [0..7]
115	10	1-255	Random Time Period, 1s-255s
116	3	0-7	Flicker Period: Fast-Slow 0..7 val
117	3	0-7	Defective Neon effects repetition time, 0 fast repetition, 7 slow repetition
120	127	0-255	Out 1 Light intensity, [1-255]
121	127	0-255	Out 2 Light intensity, [1-255]
122	127	0-255	Out 3 Light intensity, [1-255]
123	127	0-255	Out 4 Light intensity, [1-255]
124	127	0-255	Out 5 Light intensity, [1-255]
125	127	0-255	Out 6 Light intensity, [1-255]
126	127	0-255	Out 7 Light intensity, [1-255]
127	127	0-255	Out 8 Light intensity, [1-255]
128	127	0-255	Out 9 Light intensity, [1-255]
129	127	0-255	Out 10 Light intensity, [1-255]
130	127	0-255	Out 11 Light intensity, [1-255]

131	127	0-255	Out 12 Light intensity, [1-255]
132	127	0-255	Out 13 Light intensity, [1-255]
133	127	0-255	Out 14 Light intensity, [1-255]
134	127	0-255	Out 15 Light intensity, [1-255]
135	127	0-255	Out 16 Light intensity, [1-255]
136	0	0-255	Out 1, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
137	0	0-255	Out 2, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
138	0	0-255	Out 3, Effect: Bit7= 128 Random operation / 0 normal operation +

			Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
139	0	0-255	Out 4, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
140	0	0-255	Out 5, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
141	0	0-255	Out 6, Effect: Bit7= 128 Random operation / 0 normal operation +

			Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
142	0	0-255	Out 7, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
143	0	0-255	Out 8, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
144	0	0-255	Out 9, Effect: Bit7= 128 Random operation / 0 normal operation +

			Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
145	0	0-255	Out 10, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
146	0	0-255	Out 11, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
147	0	0-255	Out 12, Effect: Bit7= 128 Random operation / 0 normal operation +

			Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
148	0	0-255	Out 13, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
149	0	0-255	Out 14, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
150	0	0-255	Out 15, Effect: Bit7= 128 Random operation / 0 normal operation +

			Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
151	0	0-255	Out 16, Effect: Bit7= 128 Random operation / 0 normal operation + Bit0,1,3 = 0-Continuous, 1-Fade Lamp, 2-Fluorescent Tube, 3-Flickering Lamp, 4- Defective Neon effect
152	0	0-1	Save Last State 1-Save 0-Don't Save
160	0	0-255	F7 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F7 = 1(1): Out1 active on F7 Bit 1 = 0(0): Out2 not active on F7 = 1(2): Out2 active on F7 Bit 2 = 0(0): Out3 not active on F7 = 1(4): Out3 active on F7 Bit 3 = 0(0): Out4 not active on F7 = 1(8): Out4 active on F7

			Bit 4 = 0(0): Out5 not active on F7 = 1(16): Out5 active on F7 Bit 5 = 0(0): Out6 not active on F7 = 1(32): Out6 active on F7 Bit 6 = 0(0): Out7 not active on F7 = 1(64): Out7 active on F7 Bit 7 = 0(0): Out8 not active on F7 = 1(128): Out8 active on F7
161	0	0-255	F7 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F7 = 1(1): Out9 active on F7 Bit 1 = 0(0): Out10 not active on F7 = 1(2): Out10 active on F7 Bit 2 = 0(0): Out11 not active on F7 = 1(4): Out11 active on F7 Bit 3 = 0(0): Out12 not active on F7 = 1(8): Out12 active on F7 Bit 4 = 0(0): Out13 not active on F7 = 1(16): Out13 active on F7 Bit 5 = 0(0): Out14 not active on F7 = 1(32): Out14 active on F7 Bit 6 = 0(0): Out15 not active on F7 = 1(64): Out15 active on F7 Bit 7 = 0(0): Out16 not active on F7

			= 1(128): Out16 active on F7
162	0	0-255	F7 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F7 = 1(1): Out1 active on F7 Bit 1 = 0(0): Out2 not active on F7 = 1(2): Out2 active on F7 Bit 2 = 0(0): Out3 not active on F7 = 1(4): Out3 active on F7 Bit 3 = 0(0): Out4 not active on F7 = 1(8): Out4 active on F7 Bit 4 = 0(0): Out5 not active on F7 = 1(16): Out5 active on F7 Bit 5 = 0(0): Out6 not active on F7 = 1(32): Out6 active on F7 Bit 6 = 0(0): Out7 not active on F7 = 1(64): Out7 active on F7 Bit 7 = 0(0): Out8 not active on F7 = 1(128): Out8 active on F7
163	0	0-255	F7 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F7 = 1(1): Out9 active on F7 Bit 1 = 0(0): Out10 not active on F7 = 1(2): Out10 active on F7 Bit 2 = 0(0): Out11 not active on F7

			= 1(4): Out11 active on F7 Bit 3 = 0(0): Out12 not active on F7 = 1(8): Out12 active on F7 Bit 4 = 0(0): Out13 not active on F7 = 1(16): Out13 active on F7 Bit 5 = 0(0): Out14 not active on F7 = 1(32): Out14 active on F7 Bit 6 = 0(0): Out15 not active on F7 = 1(64): Out15 active on F7 Bit 7 = 0(0): Out16 not active on F7 = 1(128): Out16 active on F7
164	0	0-255	F8 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F8 = 1(1): Out1 active on F8 Bit 1 = 0(0): Out2 not active on F8 = 1(2): Out2 active on F8 Bit 2 = 0(0): Out3 not active on F8 = 1(4): Out3 active on F8 Bit 3 = 0(0): Out4 not active on F8 = 1(8): Out4 active on F8 Bit 4 = 0(0): Out5 not active on F8 = 1(16): Out5 active on F8 Bit 5 = 0(0): Out6 not active on F8 = 1(32): Out6 active on F8

			Bit 6 = 0(0): Out7 not active on F8 = 1(64): Out7 active on F8 Bit 7 = 0(0): Out8 not active on F8 = 1(128): Out8 active on F8
165	0	0-255	F8 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F8 = 1(1): Out9 active on F8 Bit 1 = 0(0): Out10 not active on F8 = 1(2): Out10 active on F8 Bit 2 = 0(0): Out11 not active on F8 = 1(4): Out11 active on F8 Bit 3 = 0(0): Out12 not active on F8 = 1(8): Out12 active on F8 Bit 4 = 0(0): Out13 not active on F8 = 1(16): Out13 active on F8 Bit 5 = 0(0): Out14 not active on F8 = 1(32): Out14 active on F8 Bit 6 = 0(0): Out15 not active on F8 = 1(64): Out15 active on F8 Bit 7 = 0(0): Out16 not active on F8 = 1(128): Out16 active on F8
166	0	0-255	F8 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F8 = 1(1): Out1 active on F8

			Bit 1 = 0(0): Out2 not active on F8 = 1(2): Out2 active on F8 Bit 2 = 0(0): Out3 not active on F8 = 1(4): Out3 active on F8 Bit 3 = 0(0): Out4 not active on F8 = 1(8): Out4 active on F8 Bit 4 = 0(0): Out5 not active on F8 = 1(16): Out5 active on F8 Bit 5 = 0(0): Out6 not active on F8 = 1(32): Out6 active on F8 Bit 6 = 0(0): Out7 not active on F8 = 1(64): Out7 active on F8 Bit 7 = 0(0): Out8 not active on F8 = 1(128): Out8 active on F8
167	0	0-255	F8 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F8 = 1(1): Out9 active on F8 Bit 1 = 0(0): Out10 not active on F8 = 1(2): Out10 active on F8 Bit 2 = 0(0): Out11 not active on F8 = 1(4): Out11 active on F8 Bit 3 = 0(0): Out12 not active on F8 = 1(8): Out12 active on F8 Bit 4 = 0(0): Out13 not active on F8

			= 1(16): Out13 active on F8 Bit 5 = 0(0): Out14 not active on F8 = 1(32): Out14 active on F8 Bit 6 = 0(0): Out15 not active on F8 = 1(64): Out15 active on F8 Bit 7 = 0(0): Out16 not active on F8 = 1(128): Out16 active on F8
168	0	0-255	F9 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F9 = 1(1): Out1 active on F9 Bit 1 = 0(0): Out2 not active on F9 = 1(2): Out2 active on F9 Bit 2 = 0(0): Out3 not active on F9 = 1(4): Out3 active on F9 Bit 3 = 0(0): Out4 not active on F9 = 1(8): Out4 active on F9 Bit 4 = 0(0): Out5 not active on F9 = 1(16): Out5 active on F9 Bit 5 = 0(0): Out6 not active on F9 = 1(32): Out6 active on F9 Bit 6 = 0(0): Out7 not active on F9 = 1(64): Out7 active on F9 Bit 7 = 0(0): Out8 not active on F9 = 1(128): Out8 active on F9

169	0	0-255	F9 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F9 = 1(1): Out9 active on F9 Bit 1 = 0(0): Out10 not active on F9 = 1(2): Out10 active on F9 Bit 2 = 0(0): Out11 not active on F9 = 1(4): Out11 active on F9 Bit 3 = 0(0): Out12 not active on F9 = 1(8): Out12 active on F9 Bit 4 = 0(0): Out13 not active on F9 = 1(16): Out13 active on F9 Bit 5 = 0(0): Out14 not active on F9 = 1(32): Out14 active on F9 Bit 6 = 0(0): Out15 not active on F9 = 1(64): Out15 active on F9 Bit 7 = 0(0): Out16 not active on F9 = 1(128): Out16 active on F9
170	0	0-255	F9 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F9 = 1(1): Out1 active on F9 Bit 1 = 0(0): Out2 not active on F9 = 1(2): Out2 active on F9 Bit 2 = 0(0): Out3 not active on F9 = 1(4): Out3 active on F9

			Bit 3 = 0(0): Out4 not active on F9 = 1(8): Out4 active on F9 Bit 4 = 0(0): Out5 not active on F9 = 1(16): Out5 active on F9 Bit 5 = 0(0): Out6 not active on F9 = 1(32): Out6 active on F9 Bit 6 = 0(0): Out7 not active on F9 = 1(64): Out7 active on F9 Bit 7 = 0(0): Out8 not active on F9 = 1(128): Out8 active on F9
171	0	0-255	F9 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F9 = 1(1): Out9 active on F9 Bit 1 = 0(0): Out10 not active on F9 = 1(2): Out10 active on F9 Bit 2 = 0(0): Out11 not active on F9 = 1(4): Out11 active on F9 Bit 3 = 0(0): Out12 not active on F9 = 1(8): Out12 active on F9 Bit 4 = 0(0): Out13 not active on F9 = 1(16): Out13 active on F9 Bit 5 = 0(0): Out14 not active on F9 = 1(32): Out14 active on F9 Bit 6 = 0(0): Out15 not active on F9

			= 1(64): Out15 active on F9 Bit 7 = 0(0): Out16 not active on F9 = 1(128): Out16 active on F9
172	0	0-255	F10 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F10 = 1(1): Out1 active on F10 Bit 1 = 0(0): Out2 not active on F10 = 1(2): Out2 active on F10 Bit 2 = 0(0): Out3 not active on F10 = 1(4): Out3 active on F10 Bit 3 = 0(0): Out4 not active on F10 = 1(8): Out4 active on F10 Bit 4 = 0(0): Out5 not active on F10 = 1(16): Out5 active on F10 Bit 5 = 0(0): Out6 not active on F10 = 1(32): Out6 active on F10 Bit 6 = 0(0): Out7 not active on F10 = 1(64): Out7 active on F10 Bit 7 = 0(0): Out8 not active on F10 = 1(128): Out8 active on F10
173	0	0-255	F10 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F10 = 1(1): Out9 active on F10 Bit 1 = 0(0): Out10 not active on F10

			= 1(2): Out10 active on F10 Bit 2 = 0(0): Out11 not active on F10 = 1(4): Out11 active on F10 Bit 3 = 0(0): Out12 not active on F10 = 1(8): Out12 active on F10 Bit 4 = 0(0): Out13 not active on F10 = 1(16): Out13 active on F10 Bit 5 = 0(0): Out14 not active on F10 = 1(32): Out14 active on F10 Bit 6 = 0(0): Out15 not active on F10 = 1(64): Out15 active on F10 Bit 7 = 0(0): Out16 not active on F10 = 1(128): Out16 active on F10
174	0	0-255	F10 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F10 = 1(1): Out1 active on F10 Bit 1 = 0(0): Out2 not active on F10 = 1(2): Out2 active on F10 Bit 2 = 0(0): Out3 not active on F10 = 1(4): Out3 active on F10 Bit 3 = 0(0): Out4 not active on F10 = 1(8): Out4 active on F10 Bit 4 = 0(0): Out5 not active on F10 = 1(16): Out5 active on F10

			Bit 5 = 0(0): Out6 not active on F10 = 1(32): Out6 active on F10 Bit 6 = 0(0): Out7 not active on F10 = 1(64): Out7 active on F10 Bit 7 = 0(0): Out8 not active on F10 = 1(128): Out8 active on F10
175	0	0-255	F10 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F10 = 1(1): Out9 active on F10 Bit 1 = 0(0): Out10 not active on F10 = 1(2): Out10 active on F10 Bit 2 = 0(0): Out11 not active on F10 = 1(4): Out11 active on F10 Bit 3 = 0(0): Out12 not active on F10 = 1(8): Out12 active on F10 Bit 4 = 0(0): Out13 not active on F10 = 1(16): Out13 active on F10 Bit 5 = 0(0): Out14 not active on F10 = 1(32): Out14 active on F10 Bit 6 = 0(0): Out15 not active on F10 = 1(64): Out15 active on F10 Bit 7 = 0(0): Out16 not active on F10 = 1(128): Out16 active on F10
176	0	0-255	F11 mapping, Forward move mapping, low byte

			Bit 0 = 0(0): Out1 not active on F11 = 1(1): Out1 active on F11 Bit 1 = 0(0): Out2 not active on F11 = 1(2): Out2 active on F11 Bit 2 = 0(0): Out3 not active on F11 = 1(4): Out3 active on F11 Bit 3 = 0(0): Out4 not active on F11 = 1(8): Out4 active on F11 Bit 4 = 0(0): Out5 not active on F11 = 1(16): Out5 active on F11 Bit 5 = 0(0): Out6 not active on F11 = 1(32): Out6 active on F11 Bit 6 = 0(0): Out7 not active on F11 = 1(64): Out7 active on F11 Bit 7 = 0(0): Out8 not active on F11 = 1(128): Out8 active on F11
177	0	0-255	F11 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F11 = 1(1): Out9 active on F11 Bit 1 = 0(0): Out10 not active on F11 = 1(2): Out10 active on F11 Bit 2 = 0(0): Out11 not active on F11 = 1(4): Out11 active on F11 Bit 3 = 0(0): Out12 not active on F11

			= 1(8): Out12 active on F11 Bit 4 = 0(0): Out13 not active on F11 = 1(16): Out13 active on F11 Bit 5 = 0(0): Out14 not active on F11 = 1(32): Out14 active on F11 Bit 6 = 0(0): Out15 not active on F11 = 1(64): Out15 active on F11 Bit 7 = 0(0): Out16 not active on F11 = 1(128): Out16 active on F11
178	0	0-255	F11 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F11 = 1(1): Out1 active on F11 Bit 1 = 0(0): Out2 not active on F11 = 1(2): Out2 active on F11 Bit 2 = 0(0): Out3 not active on F11 = 1(4): Out3 active on F11 Bit 3 = 0(0): Out4 not active on F11 = 1(8): Out4 active on F11 Bit 4 = 0(0): Out5 not active on F11 = 1(16): Out5 active on F11 Bit 5 = 0(0): Out6 not active on F11 = 1(32): Out6 active on F11 Bit 6 = 0(0): Out7 not active on F11 = 1(64): Out7 active on F11

			Bit 7 = 0(0): Out8 not active on F11 = 1(128): Out8 active on F11
179	0	0-255	F11 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F11 = 1(1): Out9 active on F11 Bit 1 = 0(0): Out10 not active on F11 = 1(2): Out10 active on F11 Bit 2 = 0(0): Out11 not active on F11 = 1(4): Out11 active on F11 Bit 3 = 0(0): Out12 not active on F11 = 1(8): Out12 active on F11 Bit 4 = 0(0): Out13 not active on F11 = 1(16): Out13 active on F11 Bit 5 = 0(0): Out14 not active on F11 = 1(32): Out14 active on F11 Bit 6 = 0(0): Out15 not active on F11 = 1(64): Out15 active on F11 Bit 7 = 0(0): Out16 not active on F11 = 1(128): Out16 active on F11
180	0	0-255	F12 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F12 = 1(1): Out1 active on F12 Bit 1 = 0(0): Out2 not active on F12 = 1(2): Out2 active on F12

			Bit 2 = 0(0): Out3 not active on F12 = 1(4): Out3 active on F12 Bit 3 = 0(0): Out4 not active on F12 = 1(8): Out4 active on F12 Bit 4 = 0(0): Out5 not active on F12 = 1(16): Out5 active on F12 Bit 5 = 0(0): Out6 not active on F12 = 1(32): Out6 active on F12 Bit 6 = 0(0): Out7 not active on F12 = 1(64): Out7 active on F12 Bit 7 = 0(0): Out8 not active on F12 = 1(128): Out8 active on F12
181	0	0-255	F12 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F12 = 1(1): Out9 active on F12 Bit 1 = 0(0): Out10 not active on F12 = 1(2): Out10 active on F12 Bit 2 = 0(0): Out11 not active on F12 = 1(4): Out11 active on F12 Bit 3 = 0(0): Out12 not active on F12 = 1(8): Out12 active on F12 Bit 4 = 0(0): Out13 not active on F12 = 1(16): Out13 active on F12 Bit 5 = 0(0): Out14 not active on F12

			= 1(32): Out14 active on F12 Bit 6 = 0(0): Out15 not active on F12 = 1(64): Out15 active on F12 Bit 7 = 0(0): Out16 not active on F12 = 1(128): Out16 active on F12
182	0	0-255	F12 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F12 = 1(1): Out1 active on F12 Bit 1 = 0(0): Out2 not active on F12 = 1(2): Out2 active on F12 Bit 2 = 0(0): Out3 not active on F12 = 1(4): Out3 active on F12 Bit 3 = 0(0): Out4 not active on F12 = 1(8): Out4 active on F12 Bit 4 = 0(0): Out5 not active on F12 = 1(16): Out5 active on F12 Bit 5 = 0(0): Out6 not active on F12 = 1(32): Out6 active on F12 Bit 6 = 0(0): Out7 not active on F12 = 1(64): Out7 active on F12 Bit 7 = 0(0): Out8 not active on F12 = 1(128): Out8 active on F12
183	0	0-255	F12 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F12

			= 1(1): Out9 active on F12 Bit 1 = 0(0): Out10 not active on F12 = 1(2): Out10 active on F12 Bit 2 = 0(0): Out11 not active on F12 = 1(4): Out11 active on F12 Bit 3 = 0(0): Out12 not active on F12 = 1(8): Out12 active on F12 Bit 4 = 0(0): Out13 not active on F12 = 1(16): Out13 active on F12 Bit 5 = 0(0): Out14 not active on F12 = 1(32): Out14 active on F12 Bit 6 = 0(0): Out15 not active on F12 = 1(64): Out15 active on F12 Bit 7 = 0(0): Out16 not active on F12 = 1(128): Out16 active on F12
184	0	0-255	F13 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F13 = 1(1): Out1 active on F13 Bit 1 = 0(0): Out2 not active on F13 = 1(2): Out2 active on F13 Bit 2 = 0(0): Out3 not active on F13 = 1(4): Out3 active on F13 Bit 3 = 0(0): Out4 not active on F13 = 1(8): Out4 active on F13

			Bit 4 = 0(0): Out5 not active on F13 = 1(16): Out5 active on F13 Bit 5 = 0(0): Out6 not active on F13 = 1(32): Out6 active on F13 Bit 6 = 0(0): Out7 not active on F13 = 1(64): Out7 active on F13 Bit 7 = 0(0): Out8 not active on F13 = 1(128): Out8 active on F13
185	0	0-255	F13 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F13 = 1(1): Out9 active on F13 Bit 1 = 0(0): Out10 not active on F13 = 1(2): Out10 active on F13 Bit 2 = 0(0): Out11 not active on F13 = 1(4): Out11 active on F13 Bit 3 = 0(0): Out12 not active on F13 = 1(8): Out12 active on F13 Bit 4 = 0(0): Out13 not active on F13 = 1(16): Out13 active on F13 Bit 5 = 0(0): Out14 not active on F13 = 1(32): Out14 active on F13 Bit 6 = 0(0): Out15 not active on F13 = 1(64): Out15 active on F13 Bit 7 = 0(0): Out16 not active on F13

			= 1(128): Out16 active on F13
186	0	0-255	F13 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F13 = 1(1): Out1 active on F13 Bit 1 = 0(0): Out2 not active on F13 = 1(2): Out2 active on F13 Bit 2 = 0(0): Out3 not active on F13 = 1(4): Out3 active on F13 Bit 3 = 0(0): Out4 not active on F13 = 1(8): Out4 active on F13 Bit 4 = 0(0): Out5 not active on F13 = 1(16): Out5 active on F13 Bit 5 = 0(0): Out6 not active on F13 = 1(32): Out6 active on F13 Bit 6 = 0(0): Out7 not active on F13 = 1(64): Out7 active on F13 Bit 7 = 0(0): Out8 not active on F13 = 1(128): Out8 active on F13
187	0	0-255	F13 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F13 = 1(1): Out9 active on F13 Bit 1 = 0(0): Out10 not active on F13 = 1(2): Out10 active on F13 Bit 2 = 0(0): Out11 not active on F13

			= 1(4): Out11 active on F13 Bit 3 = 0(0): Out12 not active on F13 = 1(8): Out12 active on F13 Bit 4 = 0(0): Out13 not active on F13 = 1(16): Out13 active on F13 Bit 5 = 0(0): Out14 not active on F13 = 1(32): Out14 active on F13 Bit 6 = 0(0): Out15 not active on F13 = 1(64): Out15 active on F13 Bit 7 = 0(0): Out16 not active on F13 = 1(128): Out16 active on F13
188	0	0-255	F14 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F14 = 1(1): Out1 active on F14 Bit 1 = 0(0): Out2 not active on F14 = 1(2): Out2 active on F14 Bit 2 = 0(0): Out3 not active on F14 = 1(4): Out3 active on F14 Bit 3 = 0(0): Out4 not active on F14 = 1(8): Out4 active on F14 Bit 4 = 0(0): Out5 not active on F14 = 1(16): Out5 active on F14 Bit 5 = 0(0): Out6 not active on F14 = 1(32): Out6 active on F14

			Bit 6 = 0(0): Out7 not active on F14 = 1(64): Out7 active on F14 Bit 7 = 0(0): Out8 not active on F14 = 1(128): Out8 active on F14
189		0-255	F14 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F14 = 1(1): Out9 active on F14 Bit 1 = 0(0): Out10 not active on F14 = 1(2): Out10 active on F14 Bit 2 = 0(0): Out11 not active on F14 = 1(4): Out11 active on F14 Bit 3 = 0(0): Out12 not active on F14 = 1(8): Out12 active on F14 Bit 4 = 0(0): Out13 not active on F14 = 1(16): Out13 active on F14 Bit 5 = 0(0): Out14 not active on F14 = 1(32): Out14 active on F14 Bit 6 = 0(0): Out15 not active on F14 = 1(64): Out15 active on F14 Bit 7 = 0(0): Out16 not active on F14 = 1(128): Out16 active on F14
190	0	0-255	F14 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F14 = 1(1): Out1 active on F14

			Bit 1 = 0(0): Out2 not active on F14 = 1(2): Out2 active on F14 Bit 2 = 0(0): Out3 not active on F14 = 1(4): Out3 active on F14 Bit 3 = 0(0): Out4 not active on F14 = 1(8): Out4 active on F14 Bit 4 = 0(0): Out5 not active on F14 = 1(16): Out5 active on F14 Bit 5 = 0(0): Out6 not active on F14 = 1(32): Out6 active on F14 Bit 6 = 0(0): Out7 not active on F14 = 1(64): Out7 active on F14 Bit 7 = 0(0): Out8 not active on F14 = 1(128): Out8 active on F14
191	0	0-255	F14 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F14 = 1(1): Out9 active on F14 Bit 1 = 0(0): Out10 not active on F14 = 1(2): Out10 active on F14 Bit 2 = 0(0): Out11 not active on F14 = 1(4): Out11 active on F14 Bit 3 = 0(0): Out12 not active on F14 = 1(8): Out12 active on F14 Bit 4 = 0(0): Out13 not active on F14

			= 1(16): Out13 active on F14 Bit 5 = 0(0): Out14 not active on F14 = 1(32): Out14 active on F14 Bit 6 = 0(0): Out15 not active on F14 = 1(64): Out15 active on F14 Bit 7 = 0(0): Out16 not active on F14 = 1(128): Out16 active on F14
192	0	0-255	F15 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F15 = 1(1): Out1 active on F15 Bit 1 = 0(0): Out2 not active on F15 = 1(2): Out2 active on F15 Bit 2 = 0(0): Out3 not active on F15 = 1(4): Out3 active on F15 Bit 3 = 0(0): Out4 not active on F15 = 1(8): Out4 active on F15 Bit 4 = 0(0): Out5 not active on F15 = 1(16): Out5 active on F15 Bit 5 = 0(0): Out6 not active on F15 = 1(32): Out6 active on F15 Bit 6 = 0(0): Out7 not active on F15 = 1(64): Out7 active on F15 Bit 7 = 0(0): Out8 not active on F15 = 1(128): Out8 active on F15

193	0	0-255	F15 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F15 = 1(1): Out9 active on F15 Bit 1 = 0(0): Out10 not active on F15 = 1(2): Out10 active on F15 Bit 2 = 0(0): Out11 not active on F15 = 1(4): Out11 active on F15 Bit 3 = 0(0): Out12 not active on F15 = 1(8): Out12 active on F15 Bit 4 = 0(0): Out13 not active on F15 = 1(16): Out13 active on F15 Bit 5 = 0(0): Out14 not active on F15 = 1(32): Out14 active on F15 Bit 6 = 0(0): Out15 not active on F15 = 1(64): Out15 active on F15 Bit 7 = 0(0): Out16 not active on F15 = 1(128): Out16 active on F15
194	0	0-255	F15 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F15 = 1(1): Out1 active on F15 Bit 1 = 0(0): Out2 not active on F15 = 1(2): Out2 active on F15 Bit 2 = 0(0): Out3 not active on F15 = 1(4): Out3 active on F15

			Bit 3 = 0(0): Out4 not active on F15 = 1(8): Out4 active on F15 Bit 4 = 0(0): Out5 not active on F15 = 1(16): Out5 active on F15 Bit 5 = 0(0): Out6 not active on F15 = 1(32): Out6 active on F15 Bit 6 = 0(0): Out7 not active on F15 = 1(64): Out7 active on F15 Bit 7 = 0(0): Out8 not active on F15 = 1(128): Out8 active on F15
195	0	0-255	F15 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F15 = 1(1): Out9 active on F15 Bit 1 = 0(0): Out10 not active on F15 = 1(2): Out10 active on F15 Bit 2 = 0(0): Out11 not active on F15 = 1(4): Out11 active on F15 Bit 3 = 0(0): Out12 not active on F15 = 1(8): Out12 active on F15 Bit 4 = 0(0): Out13 not active on F15 = 1(16): Out13 active on F15 Bit 5 = 0(0): Out14 not active on F15 = 1(32): Out14 active on F15 Bit 6 = 0(0): Out15 not active on F15

			= 1(64): Out15 active on F15 Bit 7 = 0(0): Out16 not active on F15 = 1(128): Out16 active on F15
196	0	0-255	F16 mapping, Forward move mapping, low byte Bit 0 = 0(0): Out1 not active on F16 = 1(1): Out1 active on F16 Bit 1 = 0(0): Out2 not active on F16 = 1(2): Out2 active on F16 Bit 2 = 0(0): Out3 not active on F16 = 1(4): Out3 active on F16 Bit 3 = 0(0): Out4 not active on F16 = 1(8): Out4 active on F16 Bit 4 = 0(0): Out5 not active on F16 = 1(16): Out5 active on F16 Bit 5 = 0(0): Out6 not active on F16 = 1(32): Out6 active on F16 Bit 6 = 0(0): Out7 not active on F16 = 1(64): Out7 active on F16 Bit 7 = 0(0): Out8 not active on F16 = 1(128): Out8 active on F16
197	0	0-255	F16 mapping, Forward move mapping, high byte Bit 0 = 0(0): Out9 not active on F16 = 1(1): Out9 active on F16 Bit 1 = 0(0): Out10 not active on F16

			= 1(2): Out10 active on F16 Bit 2 = 0(0): Out11 not active on F16 = 1(4): Out11 active on F16 Bit 3 = 0(0): Out12 not active on F16 = 1(8): Out12 active on F16 Bit 4 = 0(0): Out13 not active on F16 = 1(16): Out13 active on F16 Bit 5 = 0(0): Out14 not active on F16 = 1(32): Out14 active on F16 Bit 6 = 0(0): Out15 not active on F16 = 1(64): Out15 active on F16 Bit 7 = 0(0): Out16 not active on F16 = 1(128): Out16 active on F16
198	0	0-255	F16 mapping, Backward move mapping, low byte Bit 0 = 0(0): Out1 not active on F16 = 1(1): Out1 active on F16 Bit 1 = 0(0): Out2 not active on F16 = 1(2): Out2 active on F16 Bit 2 = 0(0): Out3 not active on F16 = 1(4): Out3 active on F16 Bit 3 = 0(0): Out4 not active on F16 = 1(8): Out4 active on F16 Bit 4 = 0(0): Out5 not active on F16 = 1(16): Out5 active on F16

			Bit 5 = 0(0): Out6 not active on F16 = 1(32): Out6 active on F16 Bit 6 = 0(0): Out7 not active on F16 = 1(64): Out7 active on F16 Bit 7 = 0(0): Out8 not active on F16 = 1(128): Out8 active on F16
199	0	0-255	F16 mapping, Backward move mapping, high byte Bit 0 = 0(0): Out9 not active on F16 = 1(1): Out9 active on F16 Bit 1 = 0(0): Out10 not active on F16 = 1(2): Out10 active on F16 Bit 2 = 0(0): Out11 not active on F16 = 1(4): Out11 active on F16 Bit 3 = 0(0): Out12 not active on F16 = 1(8): Out12 active on F16 Bit 4 = 0(0): Out13 not active on F16 = 1(16): Out13 active on F16 Bit 5 = 0(0): Out14 not active on F16 = 1(32): Out14 active on F16 Bit 6 = 0(0): Out15 not active on F16 = 1(64): Out15 active on F16 Bit 7 = 0(0): Out16 not active on F16 = 1(128): Out16 active on F16